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DFT-based controller for sag and harmonic mitigation with a series-connected compensator

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Abstract. Voltage-quality problems in power distribution networks include harmonics, voltage sags and swells and unbalances. These problems may seriously affect sensitive industrial loads causing production interruption or equipment damage. Now-a-days series voltage compensation using power electronics devices is a promising solution for these problems and the design, control and application of this type of devices have drawn much attention in the literature. In fact, comprehensive controllers for power electronics series compensator have already been proposed in the literature to tackle all those problems simultaneously. For example, repetitive controllers show very promising performance although several aspects still need closer attention. This paper proposes a different type of controller based on a Discrete Fourier Transform to minimise voltage harmonic pollution using power electronics series devices. The design process of this type of controller is straightforward regardless of the number of harmonics to be tackled. In addition, the proposed controller uses a slow sampling rate and its computational effort is relatively low. The main contributions of this paper are illustrated by simulation.

Keywords

Dynamic Voltage Restorer, Series Active Power Filter, Voltage Quality, Repetitive Controller, DFT Controller

1. Introduction

Most disconnections of industrial equipment are caused by voltage quality problems such as voltage sags and voltage harmonics. Voltage sags are often a consequence of short-circuit faults in the power system or the starting of large-rating electric motors ([1], [2]) and affect end users causing extra losses and interruptions [3]. Voltage harmonics are due to non-linear loads such as arc-furnaces and electronic rectifiers, which pour harmonic currents into the grid causing harmonic voltage drops and extra losses in power lines [4].

Dynamic Voltage Restorer (DVR) is the name used for a power electronics device conceived to restore the voltage waveform when a voltage sag occurs while Series Active Power Filter (SAPF) is the name used for the device conceived to suppress harmonic voltage distortion. Both devices share the same basic hardware equipment consisting of an electronic voltage source converter (VSC), a constant DC-link voltage, an AC filter and a coupling transformer which is series connected in the line. It is shown in [1], [5] and [6] that a series device like the one described together with a comprehensive controller can tackle all those voltage-quality problems. This type of device will be called Series Power Electronic Compensator (SPEC, for short) in the rest of the paper.

Resonant controllers are very common in power electronics to tackle harmonic problems [7] but their design is complicated because each harmonic requires the addition of a tuned block and closed-loop stability has to be addressed every time a new block is added. Repetitive controllers are also very popular in power electronics related to harmonic elimination because their basic form is easy to design and implement ([4] and [8]) but they still have several issues under investigation. In addition, in repetitive controllers, it is impossible to select which harmonics to tackle and they are prone to have problems with noise.

The Discrete Fourier Transform (DFT) is a very selective filter and has already been proposed as the core of power electronics controllers to tackle harmonics [9]. However, the resulting controller required a complex module for each harmonic to be considered leading to a heavy computational load when a long list of harmonics were dealt with and the proposal lacked of a systematic design procedure.

This paper proposes an improved DFT algorithm to track or reject harmonics which will be applied to the control of a SPEC. It will be shown that the proposed controller requires a slow sampling period and its design procedure is systematic and very straightforward. The main results will be validated by simulation using Simulink with the SimPowerSystems toolbox.

2. Controller overview

A. *Control scheme*

A SEPC is depicted in Fig. 1. The SEPC is connected between the sensitive load and the point of common coupling (PCC), where other loads may also be connected. A diode

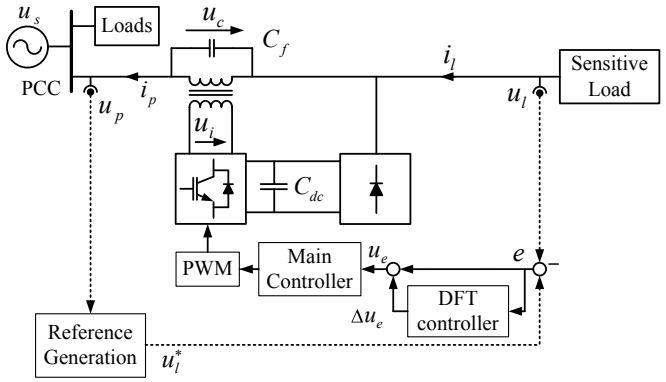

Fig. 1. SPEC controller overview

rectifier is typically used to provide the SPEC with the required power in case of voltage sag [3] and the point between the coupling transformer and the protected load has been chosen to place the rectifier. The SPEC is based on PWM voltage-source converter (VSC) connected in series with the load using a coupling transformer. The switching harmonics generated by the VSC are filtered by the transformer leakage inductance (L) and the filter capacitor (C_f).

The main objective of the SPEC is to protect the load against voltage harmonics and sags maintaining the voltage quality at the sensitive load. This is achieved by controlling the voltage injected between the mains and the load protected (u_c). The reference voltage for the controller (u_l^*) is generated with a PLL and compared with the actual load voltage (u_l), giving the load voltage error (e). To minimise this error a close-loop controller must be used. This controller typically requires two parts: a synchronous reference-frame PI controller designed to produce a fast response is appropriate to face incoming transient events from the grid such as voltage sags but due to bandwidth restrictions, the SPEC also requires an auxiliary controller to improve harmonic tracking or rejection and to tackle voltage-unbalance problems.

B. System-modelling equations

The single-phase equivalent circuit for a SPEC is depicted in Fig. 2, where Z_s models the line impedance and i_s is the supply current which consists of the sensitive-load current i_l and the rest-of-the-load current i_r. The current through the coupling transformer is i_t and i_c is the current through C_f. The current through the diode rectifier is i_d. R models the copper losses of the transformer. Assuming that $u_l(t) = u_p(t) + u_c(t)$ and ignoring i_d for simplicity because it should be small, the state-variable model for the coupling transformer and the capacitor set, using Park's transformation based on a synchronously-rotating frame, can be written as:

$$\frac{d}{dt}\boldsymbol{x} = \boldsymbol{A}\boldsymbol{x} + \boldsymbol{B}\boldsymbol{u} \tag{1}$$

where,

$$\boldsymbol{A} = \begin{bmatrix} -\frac{R}{L} & -\frac{1}{L} & \omega & 0 \\ \frac{1}{C_f} & 0 & 0 & \omega \\ -\omega & 0 & -\frac{R}{L} & -\frac{1}{L} \\ 0 & -\omega & \frac{1}{C_f} & 0 \end{bmatrix} \quad \boldsymbol{x} = \begin{bmatrix} i_t^d(t) \\ u_c^d(t) \\ i_t^q(t) \\ u_c^q(t) \end{bmatrix}$$
$$\boldsymbol{B} = \begin{bmatrix} \frac{1}{L} & 0 & 0 & 0 \\ 0 & -\frac{1}{C_f} & 0 & 0 \\ 0 & 0 & \frac{1}{L} & 0 \\ 0 & 0 & 0 & -\frac{1}{C_f} \end{bmatrix} \quad \boldsymbol{u} = \begin{bmatrix} u_i^d(t) \\ i_l^d(t) \\ u_i^q(t) \\ i_l^q(t) \end{bmatrix} \tag{2}$$

where subscripts d and q stand for direct axis and quadrature axis,respectively. The controller output is $u_i(t)$, $i_l(t)$ is a disturbance and ω is the mains frequency. Using a zero-order hold in (1), one can calculate a discrete-time model of the system [10] such as:

$$\boldsymbol{x}[k+1] = \boldsymbol{\Phi}\boldsymbol{x}[k] + \boldsymbol{\Gamma}\boldsymbol{u}[k] \tag{3}$$

with $\boldsymbol{\Phi} = e^{\boldsymbol{A}t_s}$ and $\boldsymbol{\Gamma} = \left(\int_0^{t_s} e^{\boldsymbol{A}t_s} dt\right)\boldsymbol{B}$. More precision can be obtained if the calculus delay and the delay introduced by the anti-aliasing filters are included in the discrete-time model [4]. The former is easily modelled by a one-sample delay in the command signal. The latter can also be modelled by a one-sample delay in the command because the same anti-aliasing filter is used to measure all state variables and these filters can be chosen as Bessel filters with an equivalent delay equal to one sampling period. Therefore, two new state variables are needed:

$$u_i'[k+1] = u_i[k] \tag{4}$$
$$u_i''[k+1] = u_i'[k] \tag{5}$$

C. Main controller

The dynamics of the d-axis variables and q-axis variables are coupled in (3) and a decoupling approach is very convenient. Equation (3) can be written as follows:

$$\begin{bmatrix} \boldsymbol{x_d} \\ \boldsymbol{x_q} \end{bmatrix}_{k+1} = \begin{bmatrix} \boldsymbol{\Phi_d} & \boldsymbol{0} \\ \boldsymbol{0} & \boldsymbol{\Phi_q} \end{bmatrix} \begin{bmatrix} \boldsymbol{x_d} \\ \boldsymbol{x_q} \end{bmatrix}_k + \begin{bmatrix} \boldsymbol{\Gamma_d} & \boldsymbol{0} \\ \boldsymbol{0} & \boldsymbol{\Gamma_q} \end{bmatrix} \begin{bmatrix} \boldsymbol{w_d} \\ \boldsymbol{w_q} \end{bmatrix}_k \tag{6}$$

with new input variables $\boldsymbol{w_d}$ and $\boldsymbol{w_q}$ controlling the d-axis and q-axis dynamic, respectively. These variables can be computed solving:

$$\begin{bmatrix} \boldsymbol{\Gamma_d} & \boldsymbol{0} \\ \boldsymbol{0} & \boldsymbol{\Gamma_q} \end{bmatrix} \begin{bmatrix} \boldsymbol{w_d} \\ \boldsymbol{w_q} \end{bmatrix}_k = \begin{bmatrix} \boldsymbol{0} & \boldsymbol{\Phi^c} \\ -\boldsymbol{\Phi^c} & \boldsymbol{0} \end{bmatrix} \begin{bmatrix} \boldsymbol{x_d} \\ \boldsymbol{x_q} \end{bmatrix}_k + \begin{bmatrix} \boldsymbol{0} & \boldsymbol{\Gamma^c} \\ -\boldsymbol{\Gamma^c} & \boldsymbol{0} \end{bmatrix} \begin{bmatrix} \boldsymbol{u_d} \\ \boldsymbol{u_q} \end{bmatrix}_k \tag{7}$$

Zero steady-state error for the fundamental component of the positive sequence of any state variable can be achieved by using the integral of the error in each controller (one in the d axis another one in the q axis):

$$\zeta[k+1] = \zeta[k] + t_s\left(u_l^*[k] - u_l[k]\right) \tag{8}$$

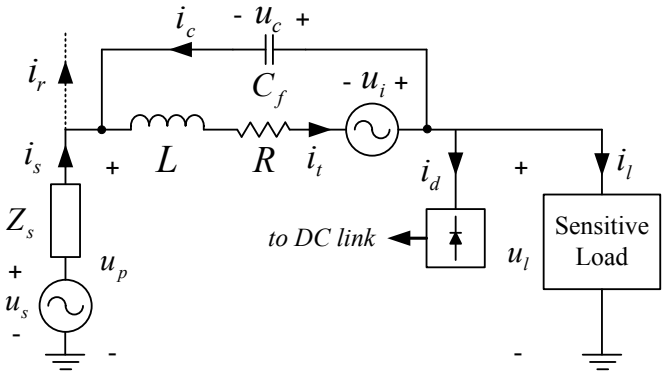

Fig. 2. Electrical model for the SPEC.

Finally, the SPEC dynamic equations for one axis with the integral controller are of the form:

$$\begin{bmatrix} i_t \\ u_c \\ u_i' \\ u_i'' \\ \zeta \end{bmatrix}_{k+1} = \begin{bmatrix} \phi_{11} & \phi_{12} & 0 & \gamma_{11} & 0 \\ \phi_{21} & \phi_{22} & 0 & \gamma_{21} & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & -t_s & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_t \\ u_c \\ u_i' \\ u_i'' \\ \zeta \end{bmatrix}_k + \begin{bmatrix} 0 & \gamma_{12} & 0 \\ 0 & \gamma_{22} & 0 \\ 1 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & t_s \end{bmatrix} \begin{bmatrix} u_i \\ i_l \\ u_c^* \end{bmatrix}_k \quad (9)$$

The main controller can be designed as a proportional state-variable feedback controller and it is depicted in Fig 3. In that figure, k_ζ is the integral-action gain, and **K** is a row vector with the rest of the gains. The controller gains can be designed using, for example, any pole-placement algorithm (see [6] and [4] for more details).

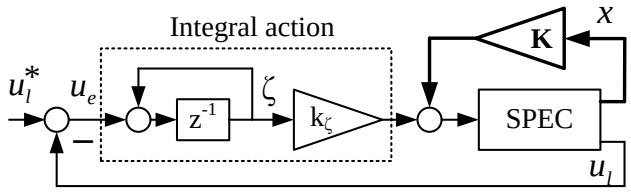

Fig. 3. SPEC main controller scheme.

D. Auxiliary controller

The main controller described before, cannot tackle voltage harmonics. An auxiliary controller is required. Moreover, if the auxiliary controller is placed as a plug-in module, the design of main and the auxiliary controllers can be carried out independently [6]. Repetitive controllers are becoming popular in power electronics as auxiliary controllers for harmonics. However, an auxiliary controller based on the DFT is proposed in this paper. Since various harmonics are going to be tracked, the use of Parks transformation into a synchronously-rotating frame is not very attractive and it has not been used here to ease the required computational load.

Fig. 4 shows the DFT controller practical implementation for one phase of the series compensator. A DFT is applied to the error signal $e(t)$ resulting in two components (real $\mathrm{Re}\{e_{(n)}\}$ and imaginary $\mathrm{Im}\{e_{(n)}\}$) for each harmonic component of the error signal. The result is a pair of numbers for each harmonic which can be treated as DC error signals and can be tackled with PI controllers ($C_{(n)}$) to eliminate the steady-state error, completely. Finally, each controller output signal ($u_{(n)}$) has to be transformed back to the time domain to reconstruct the controller output signal ($u(t)$). The ways in which the DFT and the inverse DFT can be performed are out of the scope of this paper. Notice that samples for the DFT have to be taken with a fast sampling period (t_s) to include several samples within a period of the the fastest harmonic to be considered and the same fast sampling period has to be used for the command reconstruction. However, the PI controllers applied to the DFT outputs can run with an slow sampling period (t_s').

Each of the error ($e_{(n)}$) components (real and imaginary) are related to both real and imaginary parts of the plant command ($u_{(n)}$). In order to design real- and imaginary-part independent PI controllers, it is necessary to compensate the cross-coupling terms: (a) the term relating $\mathrm{Re}\{e_{(n)}\}$ with $\mathrm{Im}\{u_{(n)}\}$, and (b) the one relating $\mathrm{Im}\{e_{(n)}\}$ with $\mathrm{Re}\{u_{(n)}\}$.

3. Proposed DFT based controller

A. Coupling matrix concept

Using the z-transform, the input($U(z)$)-output($Y(z)$) relation in a discrete-time dynamical system can be written as:

$$Y(z) = P(z)\,U(z) \quad (10)$$

and assuming a zero reference signal and unity feedback, the error ($E(z)$) can be written as:

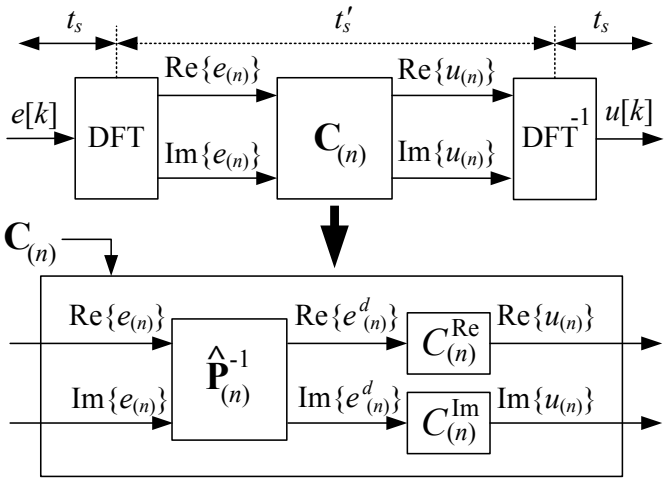

Fig. 4. DFT controller block diagram for one phase.

$$E(z) = -P(z)\,U(z) \tag{11}$$

where $P(z)$ is the plant transfer function.

In steady state each harmonic (n) in the input signal can be treated as a complex number $(U_{(n)})$ and the error in that harmonic $(E_{(n)})$ can be calculated using the plant frequency response:

$$E_{(n)} = -P_{(n)}U_{(n)} \tag{12}$$

where $P_{(n)} = P\left(z = e^{j\omega_{(n)}t_s}\right)$ and t_s is the fast sampling period.

Using matrix notation, (12) can be written as [9]:

$$\underbrace{\begin{bmatrix}\mathrm{Re}\left\{E_{(n)}\right\}\\ \mathrm{Im}\left\{E_{(n)}\right\}\end{bmatrix}}_{\mathbf{E}_{(n)}} = \underbrace{\begin{bmatrix}-\mathrm{Re}\left\{P_{(n)}\right\} & \mathrm{Im}\left\{P_{(n)}\right\}\\ -\mathrm{Im}\left\{P_{(n)}\right\} & -\mathrm{Re}\left\{P_{(n)}\right\}\end{bmatrix}}_{\mathbf{P}_{(n)}} \underbrace{\begin{bmatrix}\mathrm{Re}\left\{U_{(n)}\right\}\\ \mathrm{Im}\left\{U_{(n)}\right\}\end{bmatrix}}_{\mathbf{U}_{(n)}} \tag{13}$$

Unfortunately, (13) shows that any changes in the real (imaginary) part of the command signal $U_{(n)}$ will produce changes in both the real and the imaginary parts of the error signal $E_{(n)}$. To avoid this cross-coupling between real and imaginary axis, one can define a new error signal as:

$$\mathbf{E}^d_{(n)} = \mathbf{X}_{(n)}\mathbf{E}_{(n)} \tag{14}$$

where $\mathbf{X}_{(n)}$ is a convenient matrix. Taking (14) to (13) yields:

$$\mathbf{E}^d_{(n)} = \mathbf{X}_{(n)}\mathbf{P}_{(n)}\mathbf{U}_{(n)} \tag{15}$$

where $\mathbf{X}_{(n)}\mathbf{P}_{(n)}$ must be a diagonal matrix if real-imaginary cross-coupling is to be avoided. In fact, if the plant frequency response can be estimated as mentioned before, one can choose:

$$\mathbf{X}_{(n)} = \hat{\mathbf{P}}^{-1}_{(n)} \tag{16}$$

Obviously, the better the frequency response of the plant is known the better the decoupling will be.

B. Plant modelling using a slow sampling period

Since the DFT controller can be implemented using a slow sampling period (t'_s), a model of the plant using that sampling period is required. For example, fast and slow sampling periods can be related as:

$$t'_s = Nt_s \tag{17}$$

where N is a positive integer number.

One has then to differentiate the z-variable related to the fast sampling period (z, for example) and the z-variable related to the slow sampling period (z', for example). Using this convention, $P(z)$ would the plant model with the fast sampling period and $P'(z')$ would the plant model with the slow one. Furthermore, if t'_s is slow enough the plant can be modelled by a one-sample-period delay, approximately [11]:

$$P'(z') \approx \frac{1}{z'} \tag{18}$$

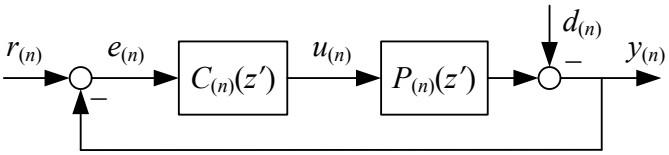

Fig. 5. Equivalent model to design the DFT controller with a slow sampling period.

C. Design of the low-sampling-rate controller

Using the simplified plant model (18) the design of an integral controller (depicted in Fig. 5) is quite straightforward and can be summarised in the following steps:

1) The closed-loop transfer function can be chosen to be

$$G'_p(z') = \frac{1-\alpha}{(z'-\alpha)} \tag{19}$$

where the parameter α is used to design the transient performance of the closed-loop system.

2) The controller can be computed for each harmonic as,

$$C_{(n)}(z') = \frac{1}{P'(z')}\frac{G'_p(z')}{1-G'_p(z')} \tag{20}$$

3) Simplifying (20) one obtains,

$$C_{(n)}(z') = \frac{(1-\alpha)\,z'}{z'-1} \tag{21}$$

which is an integral action and a gain. Notice that the controller has the same expression for all harmonics and, therefore, α can be design in the same way. The closer α is to zero, the faster the closed-loop response is.

4. Test system

A test system to validate the design proposed in previous sections has been prepared using MATLAB-SIMULINK and its SimPowerSystems toolbox. The system to be simulated in detail including the switching devices is depicted in Figure 6. The grid nominal line-to-line voltage has been set to 400 V

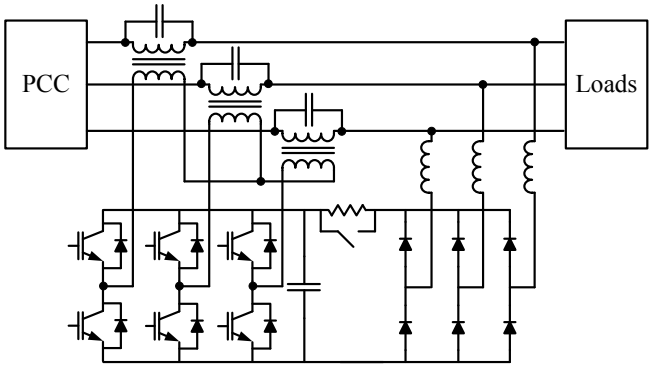

Fig. 6. Devices simulated in Simulink SimPowerSystems to test the SPEC performance.

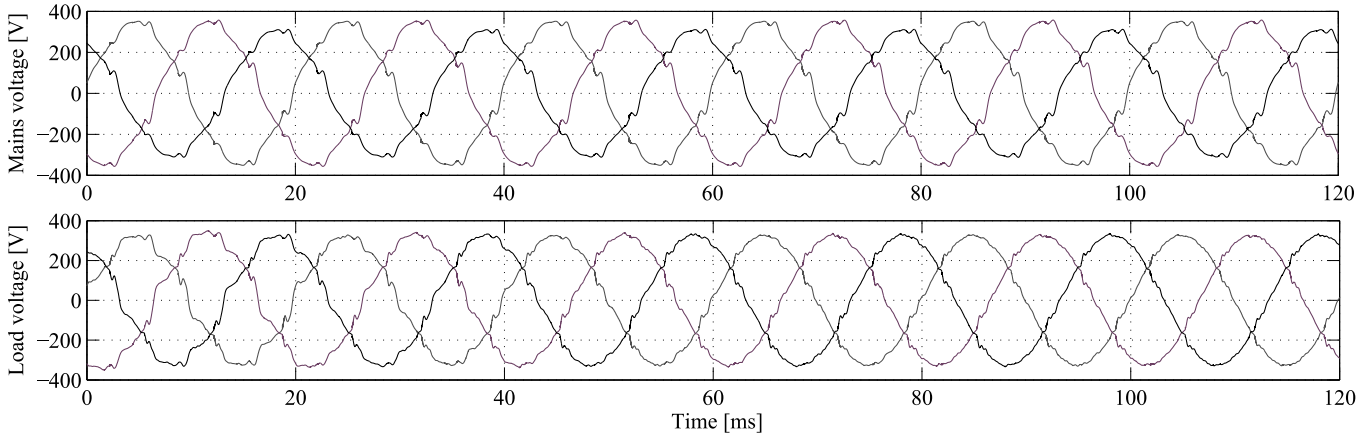

Fig. 7. Mains voltage (upper) and load voltage (lower) when the DFT controller is turned on.

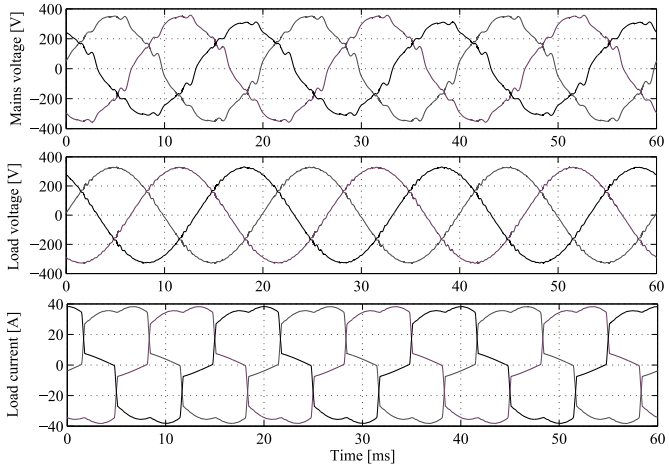

Fig. 8. SAPF steady state performance. From the top to the bottom, mains voltage, load voltage and current injected by the protected load.

and 50 Hz and the load nominal current is 30 A. The line parameters of the connection from the ideal system voltage source to the Point of Common Coupling (PCC) are $R_s = 25$ $m\Omega$ and $L_s = 1.2$ mH. The simulated load (Loads in Fig. 6) consists of an uncontrolled thyristor rectifier with $R_{dc} = 19$ Ω and $L_{dc} = 6$ mH in series in the DC side and a linear load of nominal power of 4.5 kW and 0.5 power factor. The SPEC consists of (a) a coupling transformer with unity turns ratio with the secondary in series with the line and a star-connected primary winding where the VSC is connected, (b) a filter capacitor $C_f = 27$ μF, (c) a IGBT VSC with a DC capacitor bank and an uncontrolled rectifier which is connected in parallel with the load and will help to maintain the DC link voltage. The coupling transformer has an equivalent series resistance $R = 0.05$ $m\Omega$ and a leakage inductance $L = 0.3$ mH which gives a resonant frequency for the filter equal to $1.7kHz$. The VSC switching frequency and the sampling frequency for all electrical variables has been set to 10.8 kHz.

All measures are filtered with Bessel filters, which can be modelled as a unit delay of the fast sampling period. The state feedback controller has been design with two poles at 1.8 kHz with 0.7 damping, and 3 simple poles at 4 kHz. For the DFT controller, *N* was set to 216 (one cycle of the grid frequency) and $\alpha = 0.3$ for all odd harmonics up to the 37^{th}.

5. Results

A. DFT controller performance

Fig. 7 shows the DFT controller transient response. The mains voltage (upper) contains harmonics and it is not balanced. The load voltage is depicted in the lower trace. At the beginning the SPEC is controlled only with the main controller which is able to reduce the negative-sequence voltage, but cannot filter out higher-order harmonics. The DFT controller is switched on at $t = 0$ ms. After one cycle, the effect of the SPEC is already visible. After four cycles, at $t = 80$ ms, the imbalance and the harmonics have disappeared from the load voltage.

Fig. 8 shows (from top to bottom), the mains voltage, the load voltage and the load current, in steady state. The mains voltage is unbalanced and polluted with harmonics. Part of these harmonics have been built in the simulated grid, and some others are due to the harmonic current consumed by non-linear load to be protected. The SPEC injects a voltage in series to compensate harmonics and imbalance. The load voltage is free of harmonics up to the 37^{th} one.

B. Sag mitigation

Fig. 9 illustrates the transient response on the closed-loop system when there is an unbalanced voltage sag at 40 ms. The main controller restores the voltage rapidly, but it is not able to eliminate the imbalance and the harmonics, completely. After two cycles with the auxiliary controller, the voltage is restored and the harmonics are totally rejected. Notice that part of the extra harmonic pollution during the voltage sag is due to the current consumed by the shunt rectifier of the SPEC (see Fig. 10, (d)).

Fig. 10 shows phase-a of the mains and load voltages, the DC-link voltage and the current consumed by the diode

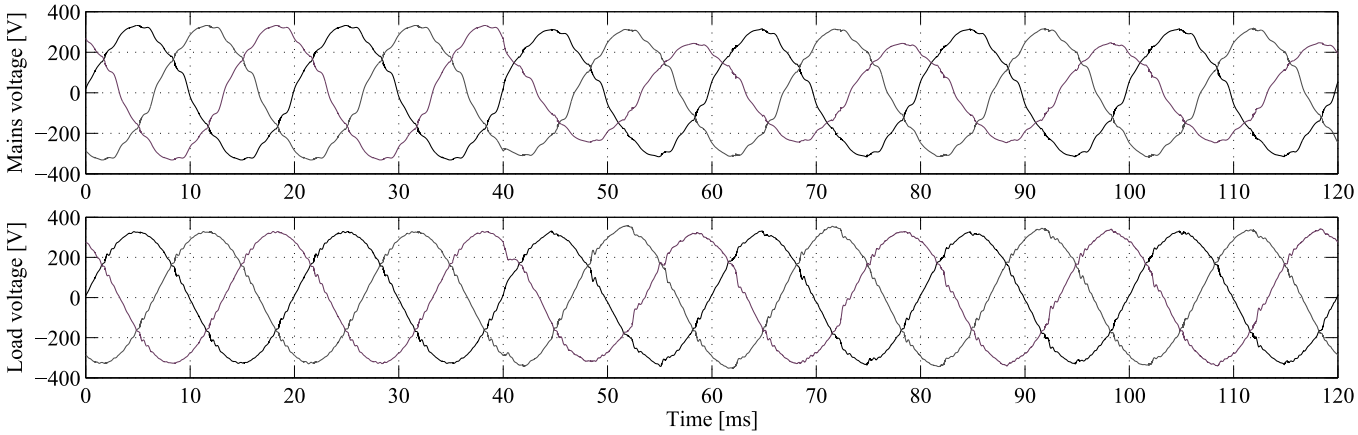

Fig. 9. Mains voltage (upper) and load voltage (lower) when there is an unbalanced voltage sag at the mains voltage

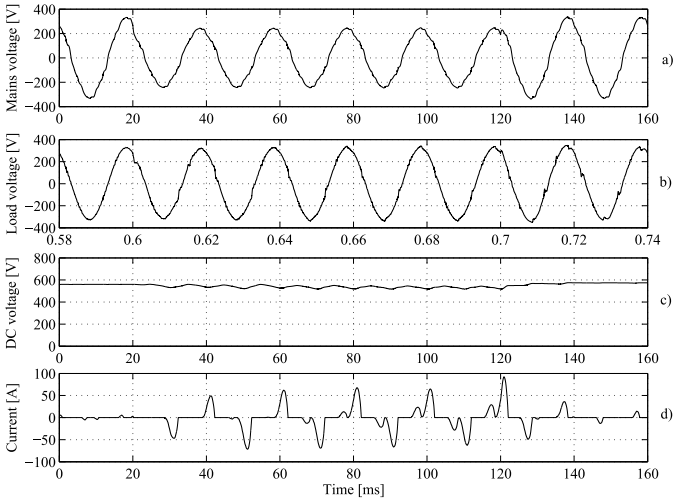

Fig. 10. (a) Phase a of the mains voltage, (b) phase a of the load voltage, (c) DC-link voltage and (d) current consumed by the diode rectifier.

rectifier. During the sag the DC link voltage oscillates and the diode rectifier consumes real (active) power. Once the sag disappears, the rectifier does not consume any current.

6. Conclusions

A slow sampling period DFT based algorithm has been proposed to reduce harmonic pollution with a series power electronics compensator (SPEC). The controller design is independent on the number of harmonics to tackle, which simplifies the design when many harmonics need to be rejected. In addition, if the slow-sampling period is selected large enough, there is no need for a sophisticated dynamical model of the system, and it is only necessary to know the frequency response at the harmonic frequencies. The proposed algorithm has been tested by simulation in a SEPC protecting a sensitive non-linear load connected to a polluted grid with unbalances and harmonic components. The use of this algorithm can be extended to many other fields like vibration control, where harmonics also takes and important role.

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